DISTRIBUTED AVERAGING ANALOG TO DIGITAL CONVERTER TOPOLOGY

Updated

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CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is a Continuation of Application No. 10/460,662, Filed: June 13, 2003, Titled: DISTRIBUTED AVERAGING ANALOG TO DIGITAL CONVERTER TOPOLOGY, Inventors: MULDER *et al.*, which is a Continuation of Application No. 10/153,709, Filed: May 24, 2002, Titled: DISTRIBUTED AVERAGING ANALOG TO DIGITAL CONVERTER TOPOLOGY, Inventors: MULDER *et al.*, which are both incorporated by reference herein.

which is now a U.S. Patent 6,628,224

BACKGROUND OF THE INVENTION

Field of the Invention

[0002] The present invention relates to analog to digital converters (ADC's), and more particularly, to various topologies for high speed analog to digital converters that use interleaving of amplifier connections to reduce parasitic capacitance.

Related Art

[0003] A subranging analog to digital converter (ADC) architecture is suitable for implementing high-performance ADC's (i.e. high speed, low power, low area, high resolution). FIG. 1 shows the generic two-step subranging architecture, comprising a reference ladder 104, a coarse ADC 102, a switching matrix 103, a fine ADC 105, coarse comparators 107, fine comparators 108 and an encoder 106. In most cases, a track-and-hold 101 is used in front of the ADC. In this architecture, an input voltage is first quantized by the coarse ADC 102. The coarse ADC 102 compares the input voltage against all the reference voltages, or against a subset of the reference voltages that is uniformly distributed across the whole range of reference